



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/064,527	07/24/2002	Chun-Hsu Lin	8992-US-PA	6640

31561 7590 09/08/2004

JIANQ CHYUN INTELLECTUAL PROPERTY OFFICE
7 FLOOR-1, NO. 100
ROOSEVELT ROAD, SECTION 2
TAIPEI, 100
TAIWAN

EXAMINER

JORGENSEN, LELAND R

ART UNIT	PAPER NUMBER
----------	--------------

2675

3

DATE MAILED: 09/08/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/064,527

Applicant(s)

LIN ET AL.

Examiner

Leland R. Jorgensen

Art Unit

2675

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 24 July 2002.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1 - 13 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1 - 13 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☒ None of:
- 1) ☒ Certified copies of the priority documents have been received.
 - 2) ☐ Certified copies of the priority documents have been received in Application No. _____.
 - 3) ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>2</u> . | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Objections

1. Claims 3, 6, 10, and 13 are objected to because of the following informalities: Each claim must end with a period. MPEP 608.01(m). Appropriate correction is required.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claims 1, 2, 4, 5, 7 – 9, 11, and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tanaka et al., USPN 6,340,961 B1, in view of Nagaoka et al., USPN 5,943,032.

Claims 1, 8, and 11

Tanaka teaches a brightness correction apparatus for a plasma display. Tanaka, col. 1, lines 9 – 14; col. 4, lines 20 – 38. An inverse γ conversion lookup unit [gamma (γ) corrector 33] receives an input signal of a currently displaying pixel and converts the input signal into a first gray scale data to be output according to an inverse γ conversion rule. Tanaka, col. 7, lines 46 – 48; col. 9, lines 59 – 67; and figure 4. An error diffusion unit [data correcting circuit 35], coupled to the inverse γ conversion lookup unit, receives the first gray scale data, and modifies the first gray scale data into a second gray scale data recorded as a display brightness error of the

Art Unit: 2675

currently displaying pixel by considering a display brightness error of a neighboring pixel of the currently displaying pixel. Tanaka, col. 7, line 52 – col. 8, line 33; col. 10, lines 1- 9; and figure 4. A gray scale lookup unit [drive circuit 3] is coupled to the error diffusion unit to receive an integral portion of the second gray scale data and to obtain a sustain pulse number of the currently displaying pixel. Tanaka, col. 8, line 55 – col. 9, line 23; and figure 4.

Although Tanaka teaches “combinations of graduation data which make actually display graduations inappropriate are registered in advance,” Tanaka does not specifically teach that plasma display has established a brightness error of ideal display brightness and actual display brightness for each gray scale. Tanaka, col. 4, lines 20 – 26. Nor does Tanaka teach putting this data in a gray scale allocation table assessable to the error diffusion unit.

Nagaoka teaches a plasma display with a brightness error of ideal display brightness and actual display brightness for each gray scale. Nagaoka, col. 9, lines 31 – 51; and figure 7.

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the pre-measured brightness error as taught by Nagaoka with the brightness correction apparatus as taught by Tanaka to enhance the display quality of the plasma display. Nagaoka invites such combination by teaching,

An object of the present invention is to provide a gray scale controlling method for a plasma display device which enhances the display quality of the plasma display device by establishing a linear relation between the gray level and the corresponding brightness.

Nagaoka, col. 2, lines 15 – 19.

Furthermore, it would have been obvious to one of ordinary skill in the art at the time of the invention to organize the brightness error as taught by Nagaoka into a gray scale allocation table accessible to the error diffusion units as such table are common and standard in the art. See

Art Unit: 2675

Nagaoka, col. 10, lines 30 – 57 which shows a table setting the number of sustain discharge pulses for each gray level.

Claims 2 and 5

Tanaka teaches an adder [correction executing circuit 50] to receive the first gray scale data to obtain the second gray scale data by summing the first gray scale data and a weighted display brightness error of the neighboring pixel. Tanaka, col. 8, lines 15 – 19; and figure 4. A brightness error lookup circuit [data reading circuit 49] is coupled to the adder to receive the integral portion of the second gray scale data and to look up a brightness error table [LUT (look-up table) 40] to obtain the brightness error of the currently displaying pixel. Tanaka, col. 8, lines 3 – 11; and figure 4. A weighted error supply circuit [pattern generator 38] is coupled to the adder and the brightness error lookup circuit to save the brightness errors of the sequentially displayed currently displaying pixel and the neighboring pixel as the display brightness errors thereof, and to weight the display brightness error of the neighboring pixel to obtain the weighted display brightness error required by the adder. Tanaka, col. 8, lines 20 – 54; and figures 4 & 5.

Claims 4 and 7

As discussed in claim 1 above, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine organize the brightness error as taught by Nagaoka into a gray scale allocation table accessible to the error diffusion unit because such table are common and standard in the art. See Nagaoka, col. 10, lines 30 – 57 which shows a table setting the number of sustain discharge pulses for each gray level. It is also obvious that that the brightness table comply with the corresponding brightness error.

Claim 9

Tanaka teaches an adder [correction executing circuit 50] to receive the first gray scale data to obtain the second gray scale data by summing the first gray scale data and a weighted display brightness error of the neighboring pixel. Tanaka, col. 8, lines 15 – 19; and figure 4. It is inherent that the correction executing circuit 50 include a subtractor because Tanaka teaches adding both positive and negative values together. The adding of negative value is done with a subtractor. A brightness error lookup circuit [data reading circuit 49] is coupled to the adder to receive the integral portion of the second gray scale data and to look up a brightness error table [LUT (look-up table) 40] to obtain the brightness error of the currently displaying pixel. Tanaka, col. 8, lines 3 – 11; and figure 4. A weighted error supply circuit [pattern generator 38] is coupled to the adder and the brightness error lookup circuit to save the brightness errors of the sequentially displayed currently displaying pixel and the neighboring pixel as the display brightness errors thereof, and to weight the display brightness error of the neighboring pixel to obtain the weighted display brightness error required by the adder. Tanaka, col. 8, lines 20 – 54; and figures 4 & 5.

Claim 12

It is inherent that the step of recording the brightness error includes recording a decimal portion of the second gray scale data.

4. Claims 3, 6, 10, and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tanaka et al., in view of Nagaoka et al. as applied to claims 1, 8, or 11 above, and further in view of Grossman et al., Advanced Engineering Mathematics (New York: Harper & Row, 1988).

Claim 3

Neither Tanaka nor Nagaoka specifically teach that the lookup table for the integral portion of the second gray scale data G and the brightness error E, and the brightness error table is established by an actual measured gray scale function of brightness $B_0(G)$ and an ideal gray scale function of brightness $B(G)$ as: $E = [(B(G) - B(G_0)) / B_0(G)] * G$.

Nagaoka, however, teaches “establishing a linear relation between the gray level and the corresponding brightness.” Nagaoka, col. 2, lines 18 – 19. See also Nagaoka, col. 19, lines 31 – 51; and figure 7. The $[(B(G) - B(G_0)) / B_0(G)]$ is the well known percent error function: the difference between the actual value and the ideal value divided by the actual value. See e.g. Grossman et al., *Advanced Engineering Mathematics* (New York: Harper & Row, 1988), p. 59.

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the percent error function with the brightness correction apparatus of Tanaka with the data taught by Nagaoka to easily calculate the error.

Double Patenting

5. Applicant is advised that should claim 4 be found allowable, claim 7 will be objected to under 37 CFR 1.75 as being a substantial duplicate thereof. When two claims in an application are duplicates or else are so close in content that they both cover the same thing, despite a slight difference in wording, it is proper after allowing one claim to object to the other as being a substantial duplicate of the allowed claim. See MPEP § 706.03(k).

Art Unit: 2675

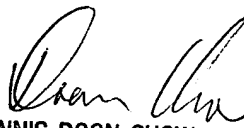
Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Leland R. Jorgensen whose telephone number is 703-305-2650. The examiner can normally be reached on Monday through Friday, 7:00 a.m. through 3:30 p.m..

The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

lrj


DENNIS-DOON CHOW
PRIMARY EXAMINER